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ART UNIT	**PAPER NUMBER**
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/027,833	WU ET AL.	
	Examiner	Art Unit	
	Stefan Stoynov	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-13,16,17 and 20-22* is/are rejected.

7)☒ Claim(s) *14,15,18,19 and 23-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

The disclosure is objected to because of the following informalities:

Re BACKGROUND:

Column 2, line 3 – the phrase "and acts" is repeated unnecessarily.

Re BRIEF DESCRIPTION OF THE DRAWINGS:

Column 4, lines 11 and 12 – the paragraph must be modified to include reference for updating the BIOS for all nodes in a multi-node partition system, thus proper correspondence to methodology shown on Figure 4.

Column 4, lines 13 and 14 – the paragraph must be modified to include reference for updating the BIOS for all nodes in multi-node partition system, thus proper correspondence to methodology shown on Figures 5a and 5b.

Figures 4, 5a, and 5b are applicable for updating the BIOS for all nodes in partitioned system upon decision at step 240, Figure 3.

Re DETAILED DESCRIPTION:

Column 10, line 3 – the word "aggregated" must be changed to "partitioned" for consistency with BRIEF DESCRIPTION OF THE DRAWINGS and methodology shown on Figures 4, 5a, and 5b.

Column 10, line 4 – the phrase "partitioned nodes" must be changed to "single partitioned node" for consistency with methodology shown on Figure 4, step 255.

Column 10, line 11 – the word "BIOS" must be changed to "SBSP" for consistency with methodology shown on Figure 4.

Appropriate correction is required.

Claim Objections

Claim 21 objected to because of the following informalities:

Column 18, line 11 – number "21" must be changed to "20".

Appropriate correction is required.

Claims 14, 15, 18, 19, and 23-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 9, and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Jacobson.

Re claim 1, Jacobson discloses a multi-node computer system comprising a plurality of nodes (FIG. 1), wherein each node comprises a processor (FIG. 6, PROCESSOR 602), and a BIOS component (column 10, lines 1-4) to store BIOS (column 9, lines 60-65 and column 10, lines 7-11) associated with the processor, wherein the BIOS in a node may be synchronized with the BIOS of another node such that BIOS coherence may be maintained between the two or more nodes (column 10, lines 12-19).

Re claim 2, Jacobson discloses the multi-node computer system (FIG. 1) of claim 1, wherein at least one BIOS component is a flash BIOS (column 10, line 3).

Re claim 9, Jacobson discloses the multiple node computer system (FIG. 1) of claim 1, wherein the computer system is a virtual multiple-processor system (column 2, lines 23-31).

Re claim 10, Jacobson discloses the multiple-node computer system (FIG. 1) of claim 9, further comprising a computer network (FIG. 1), wherein at first node is coupled (FIG. 1) to a second node across the computer network.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson.

Re claim 11, Jacobson discloses the multi-node computer system (FIG. 1) of claim 10, wherein the computer network can be any of a wide variety of communication media (column 3, lines 11-14).

Jacobson does not specifically state that the wide variety of communication media could be a wide area network (WAN). However, the use of WAN's for communication media is well known. Accordingly, the examiner takes official notice of the use of WAN's as communication media. Thus, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use a WAN for the communication media disclosed by Jacobson in order to construct a wide area network (WAN).

Claims 3, 4, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson in view of Kumar.

Re claim 3, Jacobson describes the multi-node computer system (FIG. 1) of claim 1.

Jacobson fails to disclose a memory device and the use of scalability node controller and scalable port switch in the multi-node computer system.

Kumar teaches a multi-node computer system, wherein each node further comprises a memory device (FIG.2, Memory 130) comprising a memory location operable to store data (FIG.2, memory banks 133); a scalability node controller (FIG. 2, SNC0 120) coupled (FIG. 2) to the BIOS (FIG. 2, BIOS 141) and the memory device; and a scalable port switch (FIG. 2, SPS0 275 and SPS1 276), wherein each scalable

port switch in the multi-node computer system is coupled (FIG. 2) to each scalability node controller (FIG.2, SNC0 120 and SNC1 220) in the multi-node computer system. In Kumar, the multi-node platform and method support addition or removal of a node and its components (constituent components) while the OS continues to operate (hot-plugged node) (paragraph 0016, lines 1-4). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the multi-node platform, as suggested by Kumar for the multi-node computer system disclosed by Jacobson in order to partition or aggregate the multi-node computer system.

Re claim 4, Kumar teaches the states of the scalable port switches (FIG. 2, SPS0 275 and SPS1 276) may be changed (paragraph 0043, lines 1-3) such that the nodes may be configured as a partitioned system (paragraph 0038, lines 6-9 and FIG. 6) such that each node is logically distinct, or an aggregated system (paragraph 0038, lines 9 and 10, and FIG. 5), such that all nodes are logically in a single system.

Re claim 20, Jacobson discloses a method of synchronizing plurality of BIOS (column 10, lines 12-14) for a multiple-node computer system (FIG. 1). Jacobson also describes updating the BIOS for a selected node (column 10, lines 5-7) and updating all of the nodes in the aggregated multiple-node computer system (column 1, lines 26 and 27 and column 10, lines 12-19).

Jacobson fails to disclose plurality of processors for each node, a partitioned multiple-node computer system as well as configuring the partitioning into aggregate system prior of BIOS update and restoring the partitioning system after the BIOS update.

Kumar teaches each node comprising plurality of processor (FIG. 1, processor cluster 125). Kumar also describes a partitioned multiple-node system (paragraph 0038, lines 6-9 and FIG. 6), configuring the partitioned multiple-node computer system as an aggregate (paragraph 0038, lines 9 and 10, and FIG. 5), and restoring the multiple-node computer system to a partitioned multiple-node computer system (paragraph 0038, lines 6-9 and FIG. 6). In Kumar, plurality of processors within each node (the nodes distributed across multi-node architecture) enables building larger systems with scalable performance (paragraph 0003, lines 8-13). Kumar's dynamic partitioning (splitting or merging partitions) is for reliable and efficient software upgrade in a multi-node system (paragraph 0046). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use plurality of processors within each node and the dynamic partitioning, as suggested by Kumar for the multi-node computer system disclosed by Jacobson in order to synchronize the plurality of BIOS for a partitioned multiple-node computer system.

Claims 5-8, 21, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson and Kumar, and further in view of Northcutt.

Re claim 5, Jacobson discloses the multiple-node computer system (FIG. 1) of claim 4, wherein the first processor (FIG. 6, PROCESSOR 602) located within a logical system and associated with first BIOS (column 9, lines 60-65 and column 10, lines 7-11). Jacobson also describes storing the most current version of BIOS in the memory location such that all of the processors in the logical system may be associated with the most current version of BIOS (column 10, lines 4-14).

Kumar teaches the designation of a system bootstrapping processor (SBSP) (paragraph 0035, lines 1-5). Kumar also describes a single node if the multiple-node computer system is a partitioned system (FIG. 6) or the logical system includes all of the nodes in the multiple-node computer system if the multiple-node computer system is an aggregated system (FIG. 5).

Jacobson and Kumar fail to disclose the BIOS comparison between two processors.

Northcutt teaches comparing the first BIOS to a second BIOS associated with a second processor located within the logical system to determine a most current version of BIOS (column 2, lines 26-35). In Northcutt, if the comparison of firmware associated with first and second device results in difference, the firmware of second device is updated thus ensuring firmware synchronization. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the BIOS comparison procedure, as suggested by Northcutt for the multi-node computer system disclosed by Jacobson and Kumar in order to maintain BIOS coherence between multiple processors.

Re claim 6, Kumar further teaches a server I/O hub (FIG. 2, SIOH0 and SIOH1), wherein each server I/O hub is coupled to each scalable port switch (FIG. 2, SPS0 and SPS1) in the multiple-node computer system. In Kumar, the server I/O hubs provide communications with high-speed links (paragraph 00033, lines 4-6).

Re claim 7, Kumar teaches an I/O controller hub (FIG. 1, IHC2 196), wherein each I/O controller hub is coupled to a server I/O hub (FIG. 1, SIOH 180) within the same node as the I/O controller hub. In Kumar, the I/O controller hub enables

communications with boot flash containing BIOS as well as various I/O peripherals (paragraph 0023, lines 20-23).

Re claim 8, Kumar teaches a PCI hub (FIG. 1, P64H 185) operable to coupled devices to the multi-node system, wherein each PCI hub is coupled to a server I/O hub (FIG. 1, SIO 180) located within the same node. In Kumar, the PCI hub supports communications with one or more PCI busses (paragraph 0023, lines 8-11).

Re claim 21, Jacobson discloses the method of claim 20, wherein the step of updating the BIOS for the selected node further comprises the step of synchronizing each BIOS in the selected node with the most current version of BIOS (column 10, lines 12-19).

Jacobson and Kumar fail to disclose how the BIOS version is determined prior of synchronization.

Northcutt teaches Northcutt teaches determining the most current version of BIOS (column 2, lines 26-35) for the selected node. In Northcutt, if the comparison of firmware associated with first and second device results in difference, the firmware of second device is updated thus ensuring firmware synchronization. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the BIOS comparison procedure, as suggested by Northcutt for the multi-node computer system disclosed by Jacobson and Kumar in order to synchronize the plurality of BIOS for a partitioned multiple-node computer system.

Re claim 22, Jacobson discloses the method of claim 21, wherein the step of selecting a SBSP associated with a first BIOS, wherein the SBSP is a processor in the

system (column 3, lines 7-10). Jacobson also describes placing a copy of the first BIOS in a memory location (column 9, lines 60-65).

Northcutt teaches the step of determining the most current version of BIOS further comprising the step of comparing the first BIOS to a BIOS associated with an AP to determine which BIOS is the most current version of BIOS, wherein the AP is a processor in the system that has not been selected as the SBSP (column 2, lines 26-35). In Northcutt, if the comparison of firmware associated with first and second device results in difference, the firmware of second device is updated thus ensuring firmware synchronization.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson in view of Northcutt.

Re claim 12, Jacobson discloses a method of synchronizing (column 10, lines 4-19) a plurality of BIOS for an aggregated multiple-node computer system comprising plurality of processors (FIG. 1), wherein each processor is associated with a BIOS. Jacobson also describes synchronizing each BIOS with the most current version of BIOS (column 10, lines 12-19).

Jacobson fails to disclose how the BIOS version is determined prior to synchronization.

Northcutt teaches determining the most current version of BIOS (column 2, lines 26-35). In Northcutt, if the comparison of firmware associated with first and second device results in difference, the firmware of second device is updated thus ensuring firmware synchronization. It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to incorporate the BIOS comparison procedure, as

suggested by Northcutt for the multi-node computer system disclosed by Jacobson in order to synchronize the plurality of BIOS for an aggregated multiple-node computer system.

Re claim 13, Jacobson discloses selecting a SBSP associated with a first BIOS, wherein the SBSP is a processor in the system (column 3, lines 7-10). Jacobson also describes placing a copy of the first BIOS in a memory location (column 9, lines 60-65).

Northcutt teaches the step of determining the most current version of BIOS further comprises the step of comparing the first BIOS to a BIOS associated with an AP to determine which BIOS is the most current version of BIOS, wherein the AP is a processor in the system that has not been selected as the SBSP (column 2, lines 26-35). In Northcutt, if the comparison of firmware associated with first and second device results in difference, the firmware of second device is updated thus ensuring firmware synchronization.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jacobson and Northcutt, and further in view of Kumar.

Re claim 16, Jacobson discloses a method of synchronizing (column 10, lines 4-19) a plurality of BIOS for an aggregated multiple-node computer system comprising plurality of processors (FIG. 1), wherein each processor is associated with a BIOS. Jacobson also describes synchronizing each BIOS with the most current version of BIOS (column 10, lines 12-19).

Northcutt discloses determining the most current version of BIOS (column 2, lines 26-35).

Jacobson and Northcutt fail to disclose the BIOS update in a partitioned system.

Kumar teaches a partitioned system (paragraph 0038, lines 6-9 and FIG. 6). In Kumar, the reason for dynamic partitioning (splitting or merging partitions) is for reliable and efficient software upgrade in a multi-node system (paragraph 0046). It would have been obvious to one of ordinary skill in the art at the time of applicant's invention to use the dynamic partitioning, as suggested by Kumar for the multi-node computer system disclosed by Jacobson and Northcutt in order to synchronize the plurality of BIOS for a partitioned multiple-node computer system.

Re claim 17, Jacobson discloses the method of claim 16, wherein the step of selecting a SBSP associated with a first BIOS, wherein the SBSP is a processor in the system (column 3, lines 7-10). Jacobson also describes placing a copy of the first BIOS in a memory location (column 9, lines 60-65).

Northcutt discloses the step of determining the most current version of BIOS further comprising the step of comparing the first BIOS to a BIOS associated with an AP to determine which BIOS is the most current version of BIOS, wherein the AP is a processor in the system that has not been selected as the SBSP (column 2, lines 26-35). In Northcutt, if the comparison of firmware associated with first and second device results in difference, the firmware of second device is updated thus ensuring firmware synchronization.

Allowable Subject Matter

The following is a statement of reasons for the indication of allowable subject matter:

Re claim 14, the prior art fails to disclose or suggest "updating the BIOS associated with the SBSP with a copy of the BIOS associated with the AP if the BIOS associated with the AP is more current than the first BIOS".

Re claim 18, the prior art fails to disclose or suggest "updating the BIOS associated with the SBSP with a copy of the BIOS associated with the AP if the BIOS associated with the AP is more current than the first BIOS".

Re claim 23, the prior art fails to disclose or suggest "updating the BIOS associated with the SBSP in the selected node with a copy of the BIOS associated with the AP in the selected node if the BIOS associated with the AP in the selected node is more current than the first BIOS".

Re claim 30, the prior art fails to disclose or suggest "sending an all BIOS synchronization finished status signal; and restoring the multiple-node computer system to a partitioned multiple-node system in response to the all BIOS synchronization finished status signal".

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stefan Stoynov whose telephone number is 703-305-4247. The examiner can normally be reached on 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on 703-308-1159. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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